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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,611	06/03/2005	Masaru Kuramoto	Q88048	4984

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
KIM, JAY C	

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2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/537,611	KURAMOTO ET AL.	
	Examiner	Art Unit	
	Jay C. Kim	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *12-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-21* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/3/05* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/3/05, 7/13/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Application filed June 3, 2005.

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-11, drawn to a nitride semiconductor substrate and device, classified in class 257, subclass E33.025.

II. Claims 12-21, drawn to a process for producing a nitride semiconductor substrate and device, classified in class 438, subclass 478.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, in claim 12, instead of forming a mask and then depositing a polycrystalline material on the surface of the mask, a mask material and a polycrystalline material can be deposited over the group III nitride semiconductor substrate and then be patterned to form a mask and a polycrystalline material on the surface of the mask.

2. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above

and there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:

(a) the inventions have acquired a separate status in the art in view of their different classification;

(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

3. Applicant is advised that the reply to this requirement to be complete must include (i) an election of an invention to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the

time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention.

If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 C.F.R. § 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 C.F.R. § 1.48(b) and by the fee required under 37 C.F.R. § 1.17(i).

5. During a telephone conversation with Mr. Howard Bernstein on 6/5/2007, a provisional election was made without traverse to prosecute the invention of Group I,

claims 1-11. Affirmation of this election must be made by applicant in replying to this Office action. Claims 12-21 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Examiner finds it unclear what is being referred to as "device separating plane".

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tadatomo et al. (US 6,225,650) in view of Motoki et al. (US 2003/0145783).

In regards to claim 1, Tadatomo et al. disclose a nitride semiconductor substrate (Fig. 4) comprising a base substrate (1) (col. 5, line 25 and col. 4, lines 12-15), a mask

(2) (col. 5, line 22) formed over the base substrate (1), and a semiconductor multilayer film (combined layer of 3 and 31) (col. 5, lines 25-26 and line 30) formed above the mask (2), the mask (2) being made of non-crystalline material including nitrides (col. 4, lines 27-34) and also formed into a multilayer structure (col. 4, lines 34-35).

Tadatomo et al. further disclose that a GaN crystal (1 in Figs. 9(a) and 10(a)) (col. 8, lines 57-58) can be a group III nitride semiconductor substrate for GaN crystal growth (col. 10, lines 3-9).

Tadatomo et al. differ from the claimed invention by not comprising the mask having a polycrystalline material deposited on the surface thereof.

Motoki et al. disclose a nitride semiconductor substrate (Fig. 5) where the mask (23) (SiO_2 on line 1 of [0183]) can have a polycrystalline material (polycrystalline GaN on line 2 of [0183]) deposited on the surface thereof.

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor substrate disclosed by Tadatomo et al. with the mask having a polycrystalline material deposited on the surface thereof disclosed by Motoki et al., because a multilayer mask structure for GaN crystal growth is well-known and the polycrystalline material would cause different GaN growth kinetics than a single mask structure and thus allow for better control of GaN growth.

In regards to claim 2, Tadatomo et al. in view of Motoki et al. disclose the nitride semiconductor substrate according to Claim 1.

Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that the polycrystalline material is formed from a material containing aluminum and nitrogen as essential elements.

Motoki et al. further disclose that the mask (23) can be made of polycrystalline aluminum nitride (AlN) or polycrystalline gallium nitride (GaN) ([0182]).

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor substrate disclosed by Tadatomo et al. in view of Motoki et al. with the polycrystalline AlN disclosed by Motoki et al. to make a nitride semiconductor substrate comprising polycrystalline AlN deposited on the mask, because both polycrystalline AlN and polycrystalline GaN can be used to grow high quality single crystal GaN.

In regards to claim 3, Tadatomo et al. in view of Motoki et al. disclose the nitride semiconductor substrate according to Claim 1.

Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that voids are formed on the surface of the mask having the polycrystalline material.

Motoki et al. further disclose voids (voluminous defects in voluminous defect accumulating region H in Fig. 5(a)(3)) are formed on the surface of the mask (23) having the polycrystalline material (lines 7-9 of [0299], lines 1-3 of [0420] and lines 11-13 of [0427]).

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor substrate disclosed by Tadatomo et al. in view of Motoki et al. with voids formed on the surface of the mask having the polycrystalline material disclosed by Motoki et al., because voids would be formed on a mask while growing single crystal GaN due to imperfect growth of single crystal GaN on an amorphous or polycrystalline material.

In regards to claim 4, Tadatomo et al. further disclose for the nitride semiconductor substrate according to Claim 1 that the mask (2) is provided on the surface of the group III nitride semiconductor substrate (1) (Fig. 4).

In regards to claim 5, Tadatomo et al. in view of Motoki et al. disclose the nitride semiconductor substrate according to Claim 1.

Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that the group III nitride semiconductor substrate has a dislocation density in the vicinity of the surface thereof of $1 \times 10^7/cm^2$ or less.

Motoki et al. further disclose a group III nitride semiconductor substrate (Fig. 10(5)) formed by GaN single crystal growth (Fig. 10(4)) and then polishing (line 1 of [0312]), which has a dislocation density in the vicinity of the surface thereof less than $1 \times 10^7/cm^2$ (lines 7-8 of [0316]).

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor substrate disclosed by

Tadatomo et al. in view of Motoki et al. with the low dislocation density group III nitride semiconductor substrate disclosed by Motoki et al., because the combined nitride semiconductor substrate could be used for improving device characteristics due to low dislocation density of the substrate.

In regards to claim 6, Tadatomo et al. disclose a nitride semiconductor device (Figs. 9(a), 9(b) and 10(a)) comprising a group III nitride semiconductor substrate (1) (col. 8, lines 57-58), a mask (2) (col. 4, line 8) formed over the group III nitride semiconductor substrate (1), and a semiconductor multilayer film (combined layer of 3 and k or k1) (col. 4, line 9, col. 10, lines 6-9 and col. 8, line 60) formed above the mask (2), the semiconductor multilayer film (combined layer of 3 and k or k1) including an active layer (k or k1) (col. 10, lines 6-9 and col. 8, line 60), wherein the mask (2) is made of non-crystalline material including nitrides (col. 4, lines 27-34) and also can be formed into a multilayer structure (col. 4, lines 34-35).

Tadatomo et al. differ from the claimed invention by not showing that the mask has a polycrystalline material deposited on the surface thereof.

Motoki et al. disclose a nitride semiconductor substrate (Fig. 5) where the mask (23) (SiO_2 on line 1 of [0183]) has a polycrystalline material (polycrystalline GaN on line 2 of [0183]) deposited on the surface thereof.

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor device disclosed by Tadatomo et al. with the mask having a polycrystalline material deposited on the

surface thereof, because a multilayer mask structure for GaN crystal growth is well-known and the polycrystalline material would cause different GaN growth kinetics than a single mask structure and thus allow for better control of GaN growth.

In regards to claim 7, Tadatomo et al. in view of Motoki et al. disclose the nitride semiconductor device according to Claim 6.

Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that the polycrystalline material is formed from a material containing aluminum and nitrogen as essential elements.

Motoki et al. further disclose that the mask (23) can be made of polycrystalline aluminum nitride (AlN) or polycrystalline gallium nitride (GaN) ([0182]).

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor device disclosed by Tadatomo et al. in view of Motoki et al. with the polycrystalline AlN disclosed by Motoki et al. to make a nitride semiconductor device comprising polycrystalline AlN deposited on the mask, because both polycrystalline AlN and polycrystalline GaN can be used to grow high quality single crystal GaN.

In regards to claim 8, Tadatomo et al. in view of Motoki et al. disclose the nitride semiconductor device according to Claim 6.

Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that voids are formed on the surface of the mask having the polycrystalline material.

Motoki et al. further disclose voids (voluminous defects in voluminous defect accumulating region H in Fig. 5(a)(3)) are formed on the surface of the mask (23) having the polycrystalline material (lines 7-9 of [0299], lines 1-3 of [0420] and lines 11-13 of [0427]).

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor device disclosed by Tadatomo et al. in view of Motoki et al. with voids formed on the surface of the mask having the polycrystalline material disclosed by Motoki et al., because voids would be formed on a mask while growing single crystal GaN due to imperfect growth of single crystal GaN on an amorphous or polycrystalline material.

In regards to claim 9, Tadatomo et al. further disclose for the nitride semiconductor device according to Claim 6 that the mask (2) is provided on the surface of the group III nitride semiconductor substrate (1) (Fig. 9(a)).

In regards to claim 10, Tadatomo et al. in view of Motoki et al. disclose the nitride semiconductor device according to Claim 6.

Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that the group III nitride semiconductor substrate has a dislocation density in the vicinity of the surface thereof of $1 \times 10^7/cm^2$ or less.

Motoki et al. further disclose a group III nitride semiconductor substrate (Fig. 10(5)) formed by GaN single crystal growth (Fig. 10(4)) and then polishing (line 1 of

[0312]) which has a dislocation density in the vicinity of the surface thereof less than 1 × $10^7/cm^2$ (lines 7-8 of [0316]).

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor device disclosed by Tadatomo et al. in view of Motoki et al. with the low dislocation density group III nitride semiconductor substrate disclosed by Motoki et al., because the combined nitride semiconductor device would have improved device characteristics due to low dislocation density of the substrate.

In regards to claim 11, Tadatomo et al. further disclose for the nitride semiconductor device according to Claim 6 that the mask (2 in Figs. 9(a) and 9(b)) is provided in the vicinity of a device separating plane (vertical plane separating the device in Fig. 9(b)) (col. 10, lines 14-16) of the nitride semiconductor device (Figs. 9(a) and 10(a)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jay C. Kim whose telephone number is (571) 270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew C. Landau
Primary Examiner
AU 2815
6/22/07

J. K.
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